Remarks:

Reconsideration of the application is respectfully requested.

Claims 1 - 11 are presently pending in the application.

Claims 1 and 6 have been amended.

On pages 2-4 of the above-identified Office Action, the Examiner has renewed the rejection of the previous Office Action, wherein claims 1-11 were rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U. S. Patent No. 5,781,746 to Fleck ("**FLECK**").

Applicants respectfully traverse the above rejections, as applied to the amended claims.

Applicants' previous arguments were addressed in the present Office Action, wherein it was stated, in part:

> "Contrary to Applicants' argument, even if the bus of Fleck comprises a set of wires it is clear that the term 'bus' in 'data bus' and 'control bus' is readable on the so-called 'line'. Alternatively, the term 'bus' clearly includes a 'line'. **Note that the word 'single' does not appear anywhere in the claims.** Applicants further argue that the 'buses described in Fleck are used to read and write byte or word-wide data, e.g. they are used for parallel communication. Our bidirectional line 4 is used for serial communication, (another indication that line 4 is just a single line.' **At the outset, it is noted that the words 'serial' and 'single' cannot be found in any of the claims.**" [emphasis added by Applicants]

Applicants have amended independent claims 1 and 6, herein, to recite, among other limitations, a first **single** line and a second **single** line, wherein said second **single** line is placeable in a dominant state by the logic circuit when a **serial** data transmission is to be made by the logic circuit.

As Applicants discussed in the previous response to the Office Action, **FLECK** discloses a microprocessor formed of a processing unit 2, a bus control unit 3, an internal data bus 5 and an internal control bus 6. In the Office Action, it was alleged that the internal buses 5 and 6 of **FLECK** were the same as the lines 3 and 4 in the instant application. However, **a 16 line bus and a single line** are not comparable, since a bus is formed of multiple lines (compare **FLECK** column 1, lines 21-23 and the instant application, page 3, lines 9-13).

Further, the buses described in **FLECK** are used to read and write byte or word-wide data, e.g. they are used for **parallel communication**. Applicants' bidirectional line 4 is used for **serial communication**, instead.

Regarding claims 1 and 6 of the instant application, it is presently recited that the second line is placeable in a dominant state by the logic circuit when a **serial** data transmission is to be made by the logic circuit. Simply put,

this mode or feature is not believed to be taught in Fleck as this mode applies to **serial** communications.

Furthermore, the steps according to claims 1 to 5 of the instant application are not believed to be described by **FLECK** because Applicants' claimed steps do not apply to a **parallel** communication system.

As described above, and in the Response previously filed on August 18, 2004, **FLECK** neither teaches, nor suggests, Applicants' particularly claimed first **single** line and second **single** line. Nor does **FLECK** teach or suggest that a second **single** line is placeable in a dominant state when a **serial** data transmission is to be made. These requirements are now positively recited in independent claims 1 and 6 and cannot be found in **FLECK**.

The desire to minimize the number of lines is specifically taught as an object of the present invention. Page 1, lines 9 - 13, of the instant application, state:

> "It is accordingly an object of the invention to provide a method and system for exchanging data that overcomes the hereinafore-mentioned disadvantages of the heretofore-known devices of this general type **and that minimize the required lines and connections**." [emphasis added by Applicants]

Page 3, lines 9 - 13, of the instant application describes the advantages of a **serial** implementation of the system, as follows:

> "The expenditure in terms of lines and connections is particularly low when the method according to the invention is applied, if, for the bidirectional transmission of data, **only an individual, second line** is used for the **serial** transmission." [emphasis added by Applicants]

A later mentioned plural line version is described in connection with **parallel** data communication. However, Applicants' presently claimed invention relates to that which specifically recites a **single** line when a **serial** data transmission is to occur. The busses in **FLECK** are used for **parallel** communication, **only**. As such, Applicants' presently claimed invention, is patentable over the **FLECK** reference.

It is accordingly believed to be clear that the **FLECK** reference neither teaches, nor suggests, the features of Applicants' amended claims 1 and 6. Claims 1 and 6 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 6.

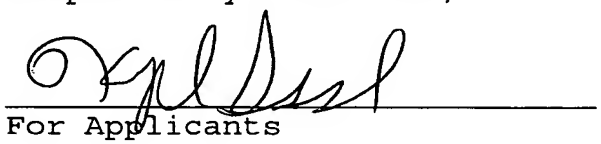
In view of the foregoing, reconsideration and allowance of claims 1 - 11 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



For Applicants

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